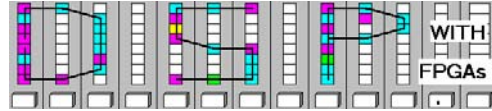


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LABORATORY
Intro. Simulink+ DSP
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LAB: INTRODUCTION TO SIMULINK AND DSP BUILDER
(10 points)

In this lab you will be introduced to the Simulink environment for the Cyclone II DSP Development board. In the **pre-lab** you will compute with “pencil-and-paper” the results you later expect in your design implementation. In the **design part** you will complete the design of a sine wave generator and become comfortable with the Simulink environment.



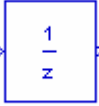
Lab Objectives

After completing this lab you should be able to

- Associate components with their library
- Understand the Simulink/DSP builder design flow
- Design and simulate a circuit using Simulink

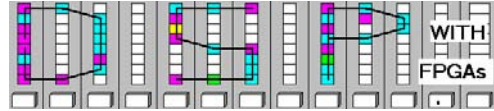
Pre-lab (3 points)

1. Download the board documentation for the Cyclone II DSP edition from Altera’s webpage or the course webpage and answer the following question.
 - a. Determine the exact name of the FPGA on the board: _____
 - b. How many LEs has the FPGA? _____
 - c. How many embedded multiplier are on the FPGA? _____
 - d. Determine the pin locations for SW2= _____ SW3 = _____ and SW4 = _____.
2. For the following elements determine the vendor library, library name and subgroup of the library:



Element	Directory	Sub-directory	Sub-directory
 D2A_1 14 Bit Unsigned	Altera DSP Builder	Boards	Stratix DSP board ...
 Scope			
 Delay			

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 Sine Wave			
 Parallel Adder Subtractor			

3. A function generator uses a LUT to store a sine table. The input to the function generator is a triangular signal and at the output an unsigned sine wave should be observed. The frequency of the sine wave should be 100 KHz. The triangle function is generated with an 17 bit (shortened) accumulator (increment M) and an 7-segment LED is used together with an extended 29 bit accumulator running at 100 MHz.

- e. Determine the period length of the 100 kHz sine wave: $T =$ _____
- f. Determine M for the 17 bit accumulator with an output frequency of 100 kHz: $M =$ _____

The sine frequency is in general much too high to be seen on the 7-segment LEDs. The MSBs of an 29 bit accumulator are used for the LED display.

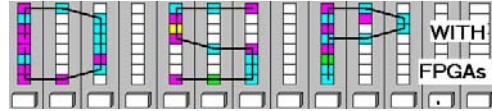
- g. Determine the LED period length for $M=1$ and 29 bit accumulator: $T =$ _____
- h. Determine the period for the 17 bit accumulator with $M=1$ $T=$ _____

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Simulink Design-lab


Follow the directions below to implement sine wave generator circuit.

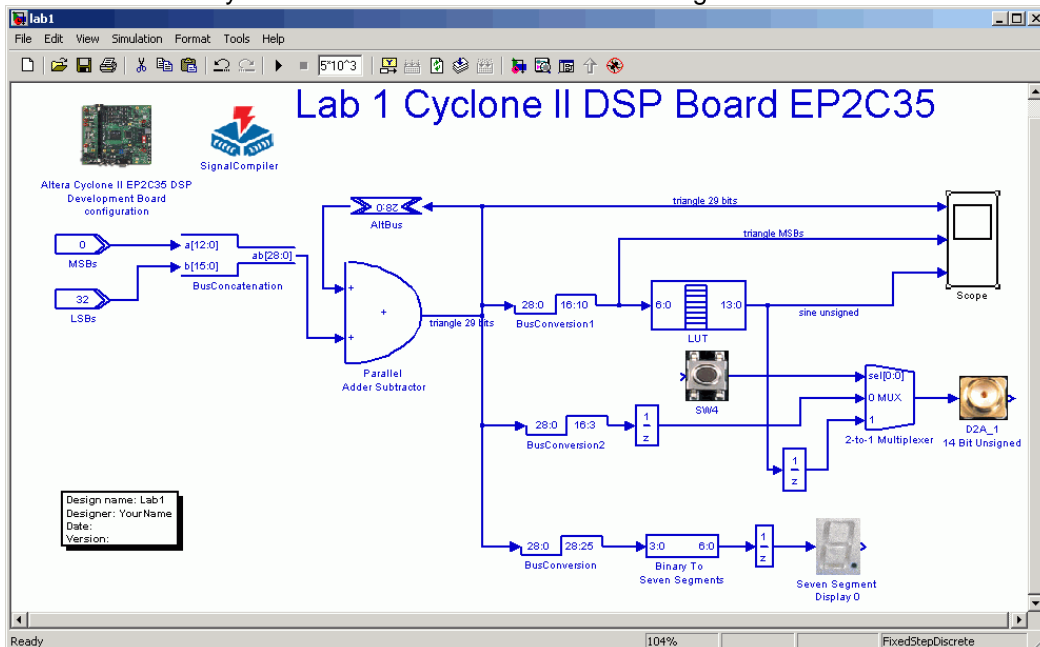
A. Getting Started

If you are in B114 or the digital logic lab:

1. On the desktop double click on **Engineering folder**.
2. Double click on **MatLab** icon  to start **MatLab**.
3. From the to top icon list in the **MatLab** window click on the **Simulink** icon  to start **Simulink**.
4. You should not save anything on the local hard disk. You will have to use an USB drive, a floppy disc, or your “mapped” home directory to save the files. Create a New Folder named **DSPwFPGAs** on your mapped network drive.

B. Compiling an Existing Design

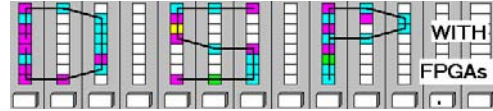
- 1) Download the file `lab1.mdl` from the class webpage and put the file in the **DSPwFPGAs** folder.
- 2) Click on the “Current Directory” selection icon  and select as current directory the **DSPwFPGAs** folder.
- 3) The files in the **DSPwFPGAs** folder are now visible in the upper left **MatLab** window. Double click on the `lab1.mdl` file and you should see after a moment the design:





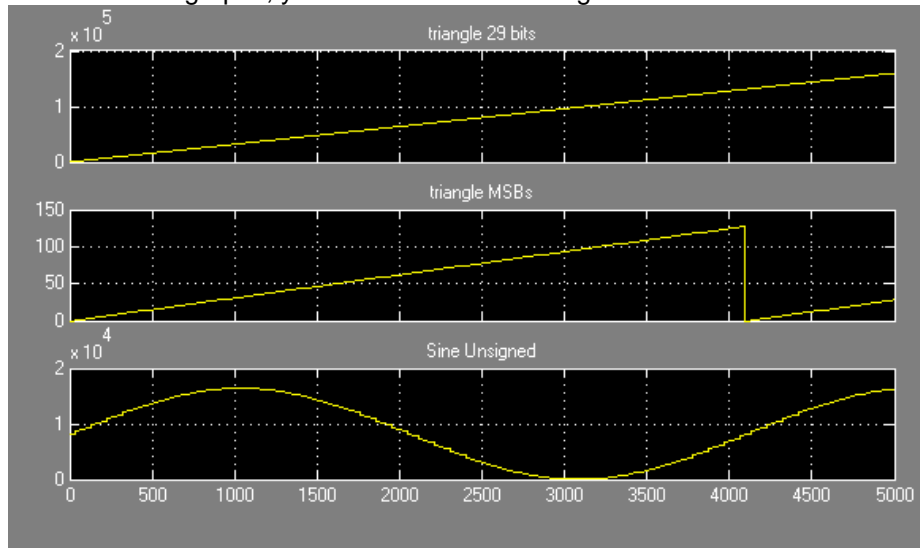
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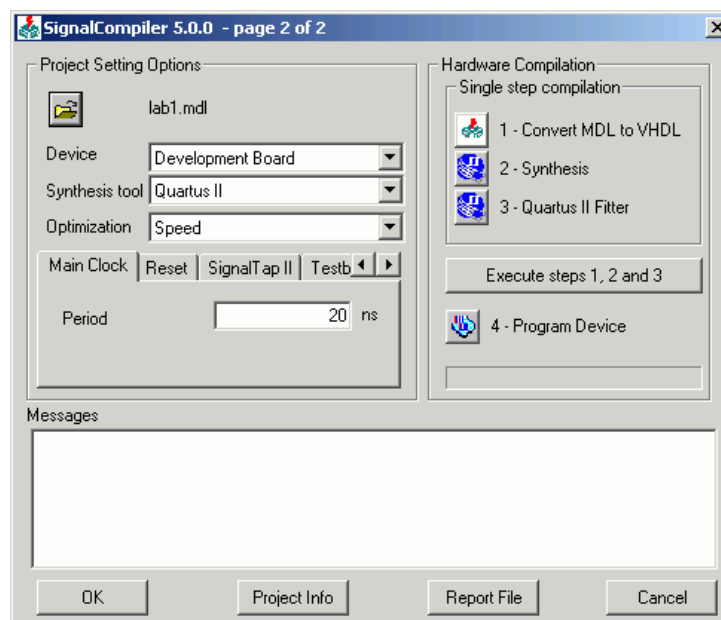
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- 4) Run the Simulation by either pressing the  icon, hitting **Ctrl+T**, or selection **Start** in the Simulation menu.
- 5) Double-click the **Scope** block and the graph window with three graphs should appear. Hit the  icon to Autoscale all the graphs, you should see something similar to:



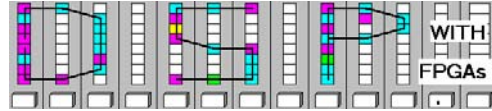
- 6) Next double-click the **SignalCompiler** block. Note That you can only compile the design on a PC that has a board, i.e. has a DSP builder license enabled.
- 7) Check the box for **Re-run update diagram to solve workspace parameters**, and then click **Analyze**.
- 8) The window below should pop up. Make sure the Reset option is set to Active Low. Click on the **Execute steps 1, 2 and 3** button. (Note: This may take a couple of minutes.)



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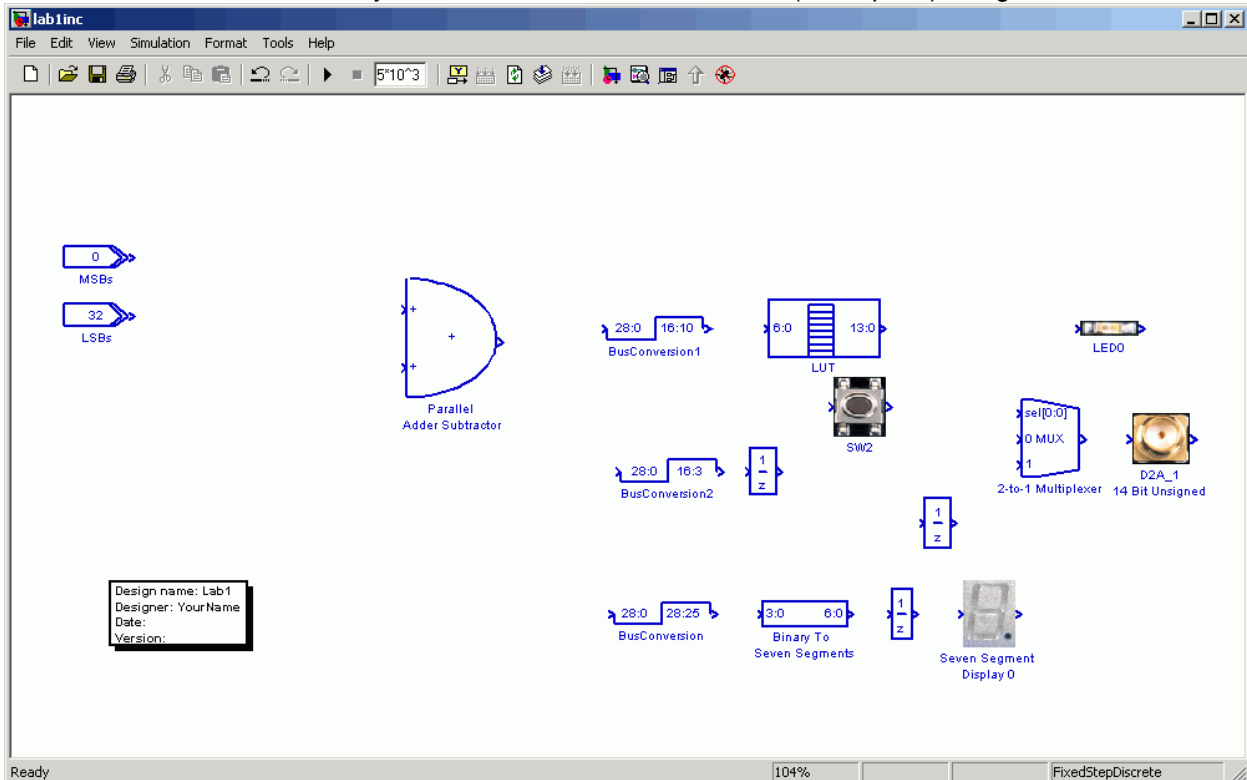
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- 9) Using the Report File determine the number of logic elements and the maximum frequency of the device:
LE = _____
MHz = _____

C. Completing The Simulink Design

- 1) Download the file `lab1inc.mdl` from the class webpage and put the file in the **DSPwFPGAs** folder.
- 2) Click on the “Current Directory” selection icon  and select as current directory the **DSPwFPGAs** folder.
- 3) The files in the **DSPwFPGAs** folder are now visible in the upper left **MatLab** window. Double click on the `lab1inc.mdl` file and you should see after a moment the (incomplete) design:

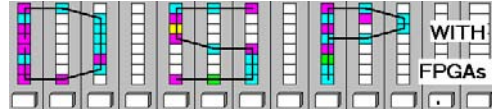


- 4) Begin completing the circuit diagram by adding the **SignalCompiler** and the **Cyclone II EP2C35 DSP Board configuration**.
 - a. Open the Library Browser icon  and select the **Altera DSP Builder** directory.
 - b. Select the **AltLab** subdirectory and find the **SignalCompiler**.
 - c. Drag the **SignalCompiler** block from the library window to your diagram.
 - d. Select the **Boards->Altera Cyclone II EP2C35 DSP Development Board** subdirectory from the **Altera** directory.
 - e. Left-click and drag the **Altera Cyclone II EP2C35 DSP Development Board configuration** block to your diagram.

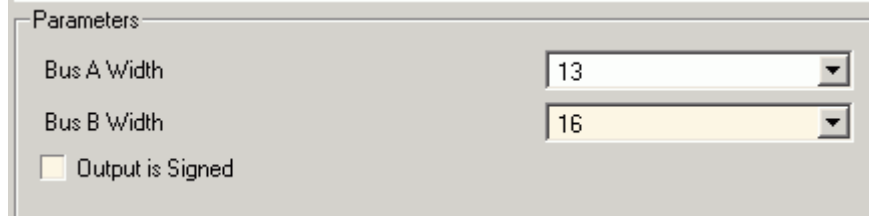
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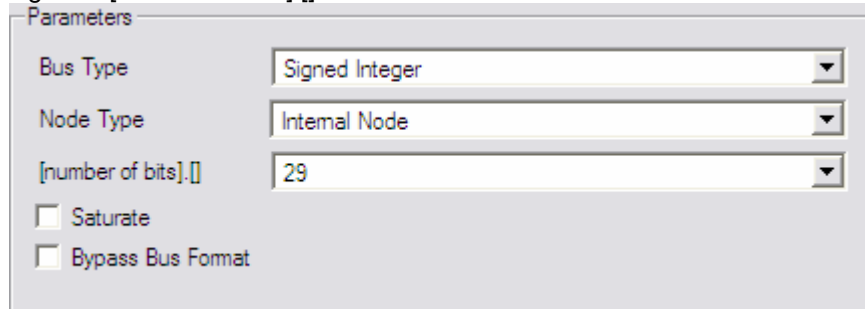


- 5) Add and connect the **BusConcatenation** block.
 - a. Find the **BusConcatenation** block in the **IO & Bus** subdirectory.
 - b. Left-click and drag the block to the diagram.
 - c. Double-click the block to view the settings and adjust them as shown below.

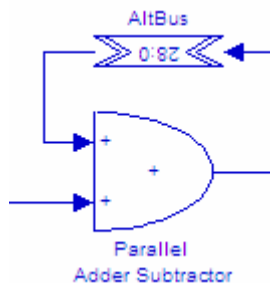


- d. Click **OK** to save the parameters.
 - e. Left-click the MSBs **Input** block, hold the **Ctrl** key, left-click on the **BusConcatenation** block, and release the **Ctrl** key. (Notice how the connection between the **Input** block and the **BusConcatenation** block is made)
 - f. Left-click the LSBs **Input** block, hold the **Ctrl** key, left-click on the **BusConcatenation** block, and release the **Ctrl** key.
 - g. Connect the **BusConcatenation** block to the **Parallel Adder Subtractor** by dragging the output arrow from the **BusConcatenation** block to the lower input of the **Parallel Adder Subtractor**. (Notice how this method can also create connections between blocks)

- 6) Connect the input and output signals for the **Parallel Adder Subtractor**.
 - a. Find the **AltBus** block in the **IO & Bus** subdirectory.
 - b. Rotate the block so that it is pointing opposite the natural direction by either hitting **Ctrl+R**, going to **Format -> Rotate Block** on the toolbar or after right clicking the block.
 - c. Place the block on the diagram and double-click the block to view the settings.
 - d. Change the [number of bits].[] box to 29 as shown below:



- e. Click **OK**, left-click the **AltBus** block and connect it to the top input of the **Parallel Adder Subtractor**.
 - f. Left-click the **Accumulator** block and connect it to the input of the **AltBus** to look like:

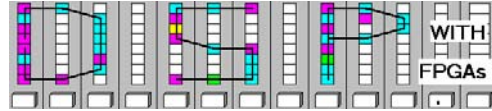


- 7) Connect all the blocks that are floating.

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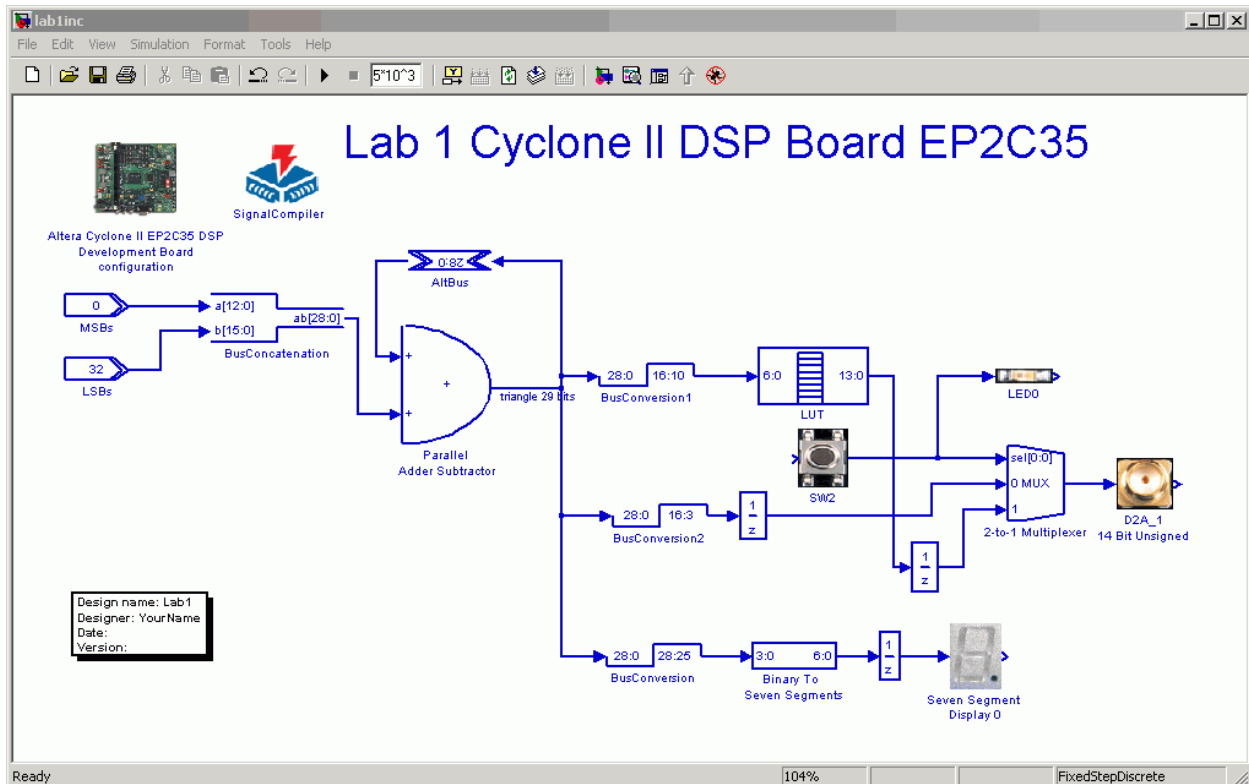
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- Start by connecting each of the **BusConcatenation** blocks to the block immediately to its right using either method described in previous steps.
- Left-click the input ports for each block and drag a wire to connect to the wire exiting the **Parallel Adder Subtractor**.
- Now all three **BusConcatenation** blocks should connect to the output of the **Parallel Adder Subtractor** and whatever block is on its right.
- Left-click the **Binary To Seven Segments** at the bottom right of the diagram and connect it to the **Delay** and then the **Delay** to the **Seven Segment Display 0** block.
- Left-click the **LUT** and connect it to **Delay** block to its bottom right, then connect the **Delay** to the 1 input to the **2-to-1 Multiplexer** block.
- Left-click the remaining disconnect **Delay** block and connect it to the 0 input of the **2-to-1 Multiplexer** block.
- Connect the **SW2** block to the sel[0:0] input on the **n-to-1 Multiplexer** and to the **LED0**. Connect the **2-to-1 Multiplexer** block to the **D2A_1 14 Bit Unsigned** block.


8) Now there is a working version that can be downloaded to the development board that should look like:



D. Simulating your design in Simulink

As you might have noticed from part B, the steps to actually downloading the model to the board take a lot of time. So it is often the case that you'll want to see the output of the schematic without downloading it to the board. In this case, a scope will be used to view the output at particular points of the schematic.

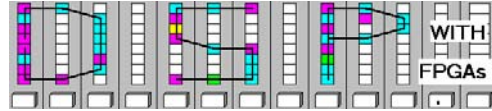
1. Add the **Scope** to the schematic.


- To add a scope, open the Library Browser by clicking on the  icon.
- Find the scope in directory found in the pre-lab.
- Drag the **Scope** block to the diagram and place it in the top right corner of the window.
- Double-click the **Scope** block to have the graph window pop up.

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- e. Click the Parameters icon .
- f. Change the number of axes to 3 as shown below:

Axes

Number of axes: 3 floating scope

Time range: auto

Tick labels: bottom axis only

- g. Click OK and return to the diagram. You should see three inputs into the **Scope**.
 - h. Click on the top input to the **Scope** and draw a wire to the connection from the **Parallel Adder Subtractor**.
 - i. Click on the middle input to the **Scope** and draw a wire to the connection between the **BusConcatenation** block and the **LUT**.
 - j. Click on the bottom input to the **Scope** and draw a wire to the connection at the output of the **LUT**.
2. Set the Simulation configuration parameters and stop time to 5000.
- a. Select **Configurations Parameters** from the **Simulation** menu from the toolbar in the **Simulink** window (or hit **Ctrl+E**). You should see the frame below in the window that appears.

Simulation time

Start time: 0.0 Stop time: 5*10³

Solver options

Type: Fixed-step Solver: discrete (no continuous states)

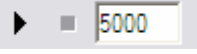


Periodic sample time constraint: Unconstrained

Fixed-step size (fundamental sample time): auto

Tasking mode for periodic sample times: SingleTasking

Higher priority value indicates higher task priority

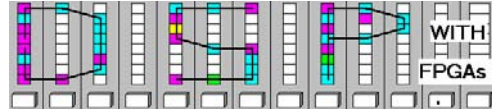
Automatically handle data transfers between tasks

- b. Change the Type to be Fixed-step and Solver should be set to discrete (no continuous states).
 - c. Change the Stop time to read 5000 or $5 \cdot 10^3$. Click OK and the **Simulink** window should show the stop time as seen in (d).
 - d. The simplest way to set the simulation stop time is to change the value in the **Simulink** window, , appropriately.
3. Run the Simulation by either hitting the  icon, hitting **Ctrl+T**, or selection **Start** in the Simulation menu.
4. Double-click the **Scope** block and the graph window with three graphs should appear. Hit the  icon to Autoscale all the graphs. Verify that you get two triangle and a sin function as in pat B.

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5. Now the values for the LSBs **Input** block have been adjusted such that the Sine Unsigned waveforms will have the number of samples T per period as specified in the following:

T = 4000, LSBs = _____

T = 1000, LSBs = _____

T = 700, LSBs = _____

E. Compiling Your Design using SignalCompiler

Complete steps 4 – 6 from part B where the LSBs **Input** block is equal to the value M you computed in the Prelab for an output 100 kHz frequency.

From the Report File:

LEs = _____

MHz = _____

F. Download your design to the FPGA board

Once you have completed compiling your model, you can now download it to the board.

1. Have a board at computer or move to one that does.
2. Power up the board if needed by plugging it in and flipping the switch next to the power supply port so that a blue LED is lit.
3. Once the compilation steps are done, the Program Device button will become available. If not, check the design for error and re-run the compilation steps.
4. Watch the output of the D2A output with an oscilloscope or the 7-segment LEDs in case you do not have an oscilloscope connected to the board. Go back and change the values of the **LSBs** to M=1 so that the characteristics of the device can be viewed from the seven-segment display. (Note: Updating and re-running all the compilation steps is necessary.)
5. Show the lab TA your working FPGA board design.

F. Deliverables

- 1) Solve the problems of the pre-lab. (3 points).
- 2) Print the completed MDF file `lab1inc.mdl` and the Simulink simulation (7 points).

Make sure your name and SS is on all pages you turn in!