Lastname: ____________________

5Digit SS:___________________

LABORATORY
FIR Filter

LAB FIR: INTRODUCTION TO FIR FILTER
(10 points)

In this lab you will be introduced to the design for FIR filters. Filters are one of the most important DSP object and are used most of the time to select a specific frequency band of the signal. FIR filter have low quantization sensitivity, simple structures, and can easily be made be of linear phase.
In the **pre-lab** you will compute with "pencil-and-paper" the results you later expect in your design implementation. In the **design part** you will design you will design a halfband-filter using direct coefficient coding and reduced adder graph design.

Lab Objectives

After completing this lab you should be able to

- Design and simulate an moving average filter
- Understand the difference between direct and transposed form FIR filters
- Design and simulate a reduced adder graph FIR filter using Simulink

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Pre-lab (3 points)

For a moving average filter with K-taps determine the output scaling that the overall gain of the filter is 1.

Gain for the output = _________________.

What output scaling is required for a 4-tap MAF?

Gain for 4-tap MAF = _________________.

1. For a 3-tap moving average filter determine the output values y[n] =(x[n]+…+x[n-2])/3 for the input values x[n]. Assume zero values x[n],y[n]=0 for 0<n and n>8.

n=	**0**	**1**	**2**	**3**	**4**	**5**	**6**	**7**	**8**
x[n]=	**1**	**-2**	**4**	**3**	**2**	**3**	**0**	**3**	**1**
y[n]=									

What is your guess (i.e. sine;cosine;triangular;rectangular) regarding the original signal x[n]?

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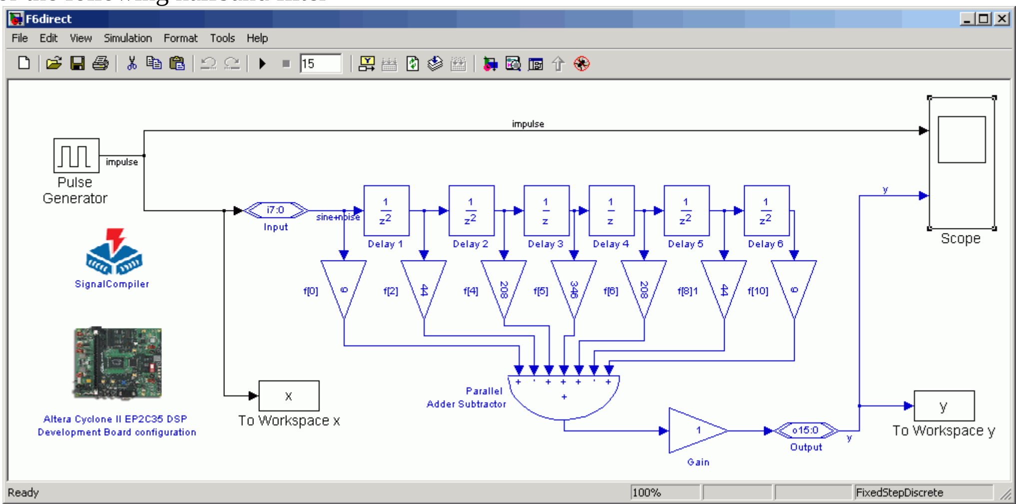
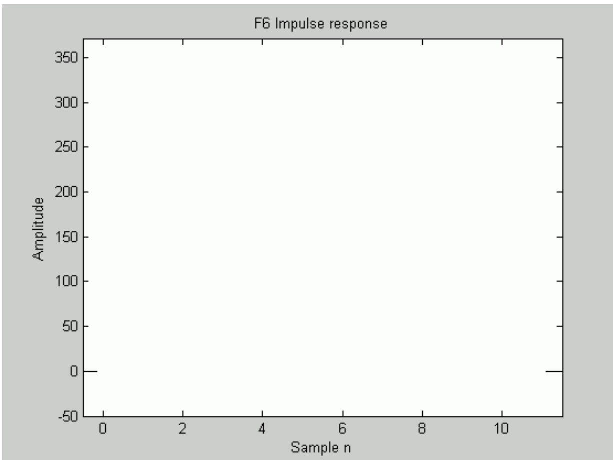
2. For the following halfband filter



draw the impulse response using "step functions"



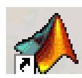
3. Determine for the length-11 half band filter F5 with coefficient f[0]=f[10]=3; f[2]=f[8]=-25; f[4]=f[6]=150; and f[5]=256 the reduced adder graph. Hint: 150=2*(3*(3*8+1)).

Simulink Design-lab

Follow the directions below to implement a moving average and halve band filter circuit.

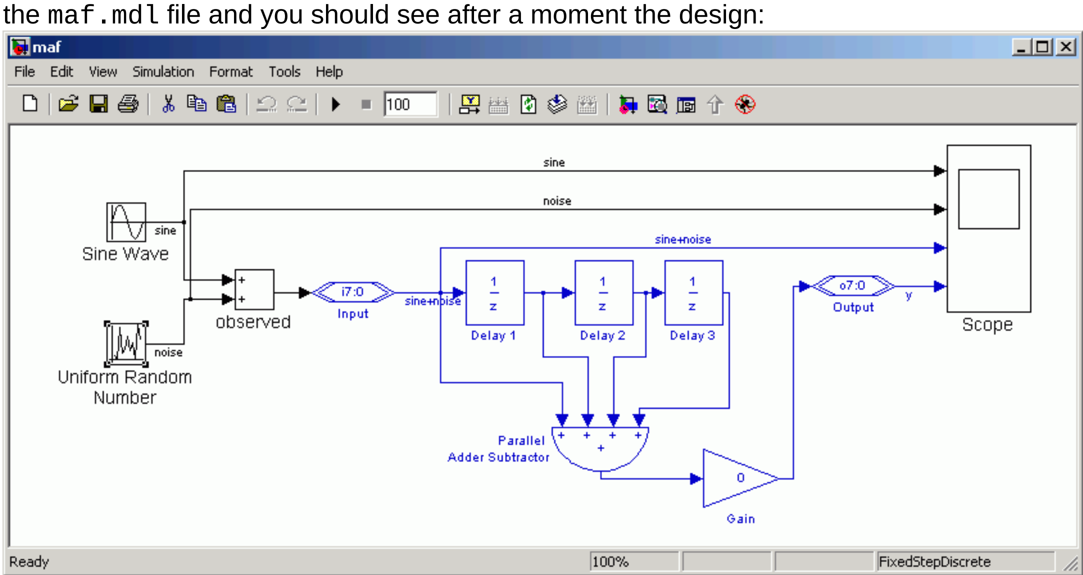
A. Getting Started

If you are in B114 or the digital logic lab:

1. On the desktop double click on **Engineering folder**.
2. Double click on **MatLab** icon  to start **MatLab**.
3. From the to top icon list in the **MatLab** window click on the **Simulink** icon  to start **Simulink.**
4. You should not save anything on the local hard disk. You will have to use a Zip, a floppy disc, or your “mapped” home directory to save the files. Create a New Folder named **DSPwFPGAs** on your mapped network drive.

B. Compiling an Existing Moving average Design

1. Download the file `maf.mdl` from the class webpage and put the file in the **DSPwFPGAs** folder.
2. Click on the “Current Directory” selection icon and select as current directory the **DSPwFPGAs** folder.
3. The files in the **DSPwFPGAs** folder are now visible in the upper left **MatLab** window. Double click on the `maf.mdl` file and you should see after a moment the design:



4. Modify the gain that the overall gain of the system is 1. Carefully choose the number of integer and fractional bits in the gain block. Verify the correct function via Simulink simulation.

5. The Random noise generator amplitude is initially set to 10. Increase the amplitude in steps of 5. What is the maximum amplitude of the noise the MAF can tolerate such that the output is clearly a sine function: (print the simulation of the largest amplitude without distortion and the simulation with distortion)

   Maximum Noise Amplitude = ____________________

C. Simulating the F5 direct form Filter

1. Download the file `F5direct.mdl, showfft.m` from the class webpage and put the file in the **DSPwFPGAs** folder.

2. Simulate the design. (Print out to turn in.)

3. Use the function `showfft(x)` and `showfft(y)` provided to "measure" the amplitude of the "noise" sine component before and after filtering. Compare the results to the results using the 4-tap moving average filter.

4. Compile the design using **Signal Compiler** and determine

   LCs = ________________

   MHz = ________________

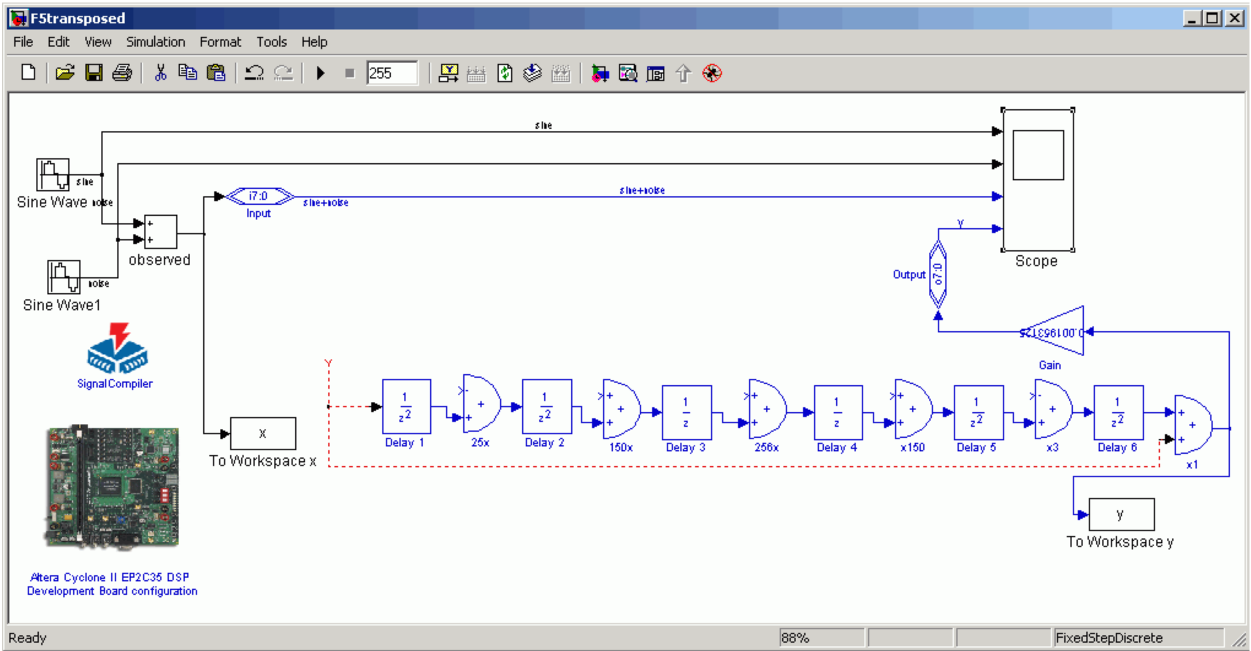
   from the report files.

D. Complete the R5 RAG Simulink Design

The direct form FIR filter can be optimized in several ways. First, we use a constant coefficient multiplier block (called gain), instead of the general purpose multiplier. We use the transposed FIR form to reduce the adder delay. Finally we can combine the coefficient using the reduced adder graph you have developed in the pre-lab.

1. Download the file `F5transposed.mdl` from the class webpage and put the file in the **DSPwFPGAs** folder.

2. Complete the design, i.e. add the reduced adder graph you developed in the pre-lab to implement the coefficients array. (Print out to turn in.)



3. Simulate the design in Simulink and verify the functionality. (Print out to turn in.)

4. Compile the design using **Signal Compiler** and determine

   LCs = ________________

   MHz = ________________

   from the report files.

5. Compare this design with the direct form design `f5direct.mdl`. Determine the improvement:

Improvement LCs = _______________%

Improvement MHz = ________________%

F. Deliverables:

1. Solve the problems of the pre-lab. (3 points).
2. Print the MDF file and the Simulink simulations (7 points).

Make sure your name and SS is on all pages you turn in!