

**Digital anti-windup PI controllers for variable-speed motor drives using FPGA and stochastic theory**

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*Abstract* – The windup phenomenon occurs when the output of a proportional-integral (PI) controller is saturated, which results in performance degradation or even instability. In this paper, three new anti-windup algorithms are proposed for a digital PI speed controller to improve the control performance of variable-speed motor drives. These designs are implemented in a Field Programmable Gate Arrays (FPGA) device and stochastic theory is employed to enhance the computational capability of FPGA. Compared with conventional digital anti-windup techniques, the proposed methods offer several advantages: large dynamic range, easy digital design, minimizing the scale of digital circuits, re-configurability, and direct hardware implementation, while maintaining high control performance. The developed controllers are applied to the speed control of a field-oriented controlled induction motor drive using a hardware-in-the-loop test bench. The improved speed responses confirm the effectiveness of the proposed anti-windup schemes.

*Index Terms* — Field Programmable Gate Arrays, anti-windup, PI control, variable-speed motor drive, stochastic theory

## I. INTRODUCTION

In the speed control of variable-speed motor drives, a large step change in the speed command will cause the generated current command from a proportional-integral (PI) speed controller to exceed the prescribed maximum value, which is determined by the converter protection, the magnetic saturation, and the motor overheating. Thus a saturator is applied which introduces a non-linearity into the system. This phenomenon is called integrator windup and can lead to large overshoot, long settling time, and even unstable closed-loop systems [1] since the parameters of the PI speed controller is normally designed in a linear region, ignoring the saturation nonlinearity. In an attempt to overcome the windup phenomenon, a number of anti-windup techniques have been proposed in the literature, for example [2-6]. Currently, digital implementations of anti-windup PI controllers are based on a microprocessor or DSP [7]. Hardware solutions such as Field Programmable Gate Arrays (FPGA) have advantages in price, execution speed and flexibility, but are restricted for their poor calculation ability [8] and low available number of logic gates in a typical FPGA [9]. Stochastic arithmetic provides an effective means of enhancing the computational capability of FPGA with the same logic gates density [10]. This is an efficient implementation approach that uses simple digital logic circuits but has the advantage of significantly reducing the circuit complexity compared with the traditional digital implementation approach.

In this paper, new anti-windup PI controllers are proposed and implemented in a FPGA device using stochastic arithmetic. The developed designs provide solutions to enhance the computational capability of FPGA and offer several advantages: large dynamic range, easy digital design, minimization of the scale of digital circuits, reconfigurability, and direct hardware implementation while maintaining the high control performance of traditional anti-windup techniques. The improved speed responses measured from a hardware-in-the-loop test bench confirm the effectiveness of the proposed anti-windup schemes.

## II. PROPOSED STOCHASTIC ANTI-WINDUP PI CONTROLLERS

### A. Introduction of stochastic integrator

The digital integrator can be expressed in  $y(n) = x(n) + y(n-1)$ . Fig.1 (a) presents the traditional accumulator design of a digital integrator. A large register holds the previous output of the integrator and sends the one-step time-delayed output signal back to the adder to perform the integration function. Fig.2 (b) shows an alternative

approach to digital integration using stochastic arithmetic. The stochastic digital integrator has two elements: a signal value to frequency converter (randomization block) and an up-down (pulse) counter. In the randomization process shown in Fig.2, the value of the input signal  $X$  is equal to the number of occurrence of '1' in the output bit stream. If  $p$  is the probability to have a bit '1' on any position in the bit stream, then the value of the input signal is given by the expression  $x = (2p - 1) \cdot c$ , where  $c$  is a constant and the input  $x$  must be in  $[-c, c]$ . For example, if  $x=c$ , then the output bit stream will be all '1's and if  $x=-c$ , the output bit stream will be all '0's. After this process, the Up/Down counter accumulates the incoming pulses and performs the integration function.

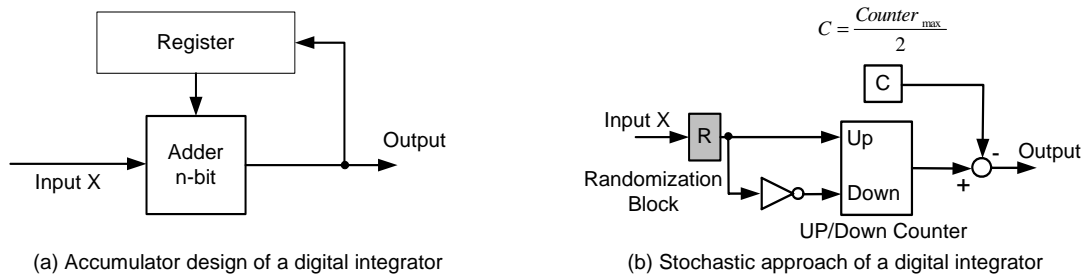


Fig.1 Block diagram of the traditional and stochastic integration schemes

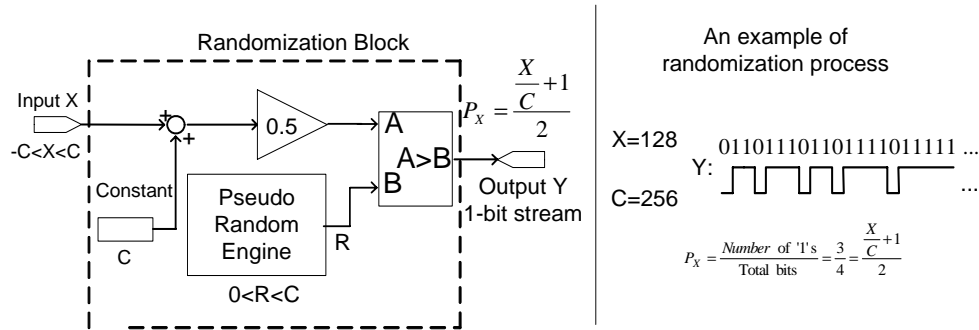


Fig.2 Randomization process and an example

Compared with the traditional approach of implementing digital integration, the stochastic method has a larger dynamic range and gets rid of the n-bit adder that contains tens of logic gates. Although the randomization process requires extra digital resources for the pseudo random engine and the comparator, these resources can be shared if many digital integrators are employed in the same digital Integrated Circuits (ICs).

### B. Proposed anti-windup strategies based on the stochastic integrator

To date, most developed anti-windup strategies can be classified as either a conditional integration scheme, a back-calculation scheme or a hybrid scheme, as illustrated in Fig.3 (a), (b), and (c), respectively. The conditional integration scheme is reported as the most popular anti-windup strategy due to its simplicity. To avoid the

accumulation of errors, the integral action turns off when the output signal reaches the saturator's limit which is not able to change the control performance any more. In the back-calculation scheme, the integral term is reduced in magnitude when the output saturates. The tuning parameter  $K_a$  decides the decrease in the rate of the integral term's magnitude. The hybrid scheme, as shown in Fig.3(c), combines the previous two approaches. When the tuning parameter  $K_a$  is chosen to be small, the scheme works as the conditional integration scheme. On the other hand, the hybrid scheme goes to the back-calculation scheme when  $K_a$  is set to be large. Compare with the conditional integration scheme. The last two schemes suffer from complicated and time-consuming design processes in optimizing the free parameters  $K_a$ .

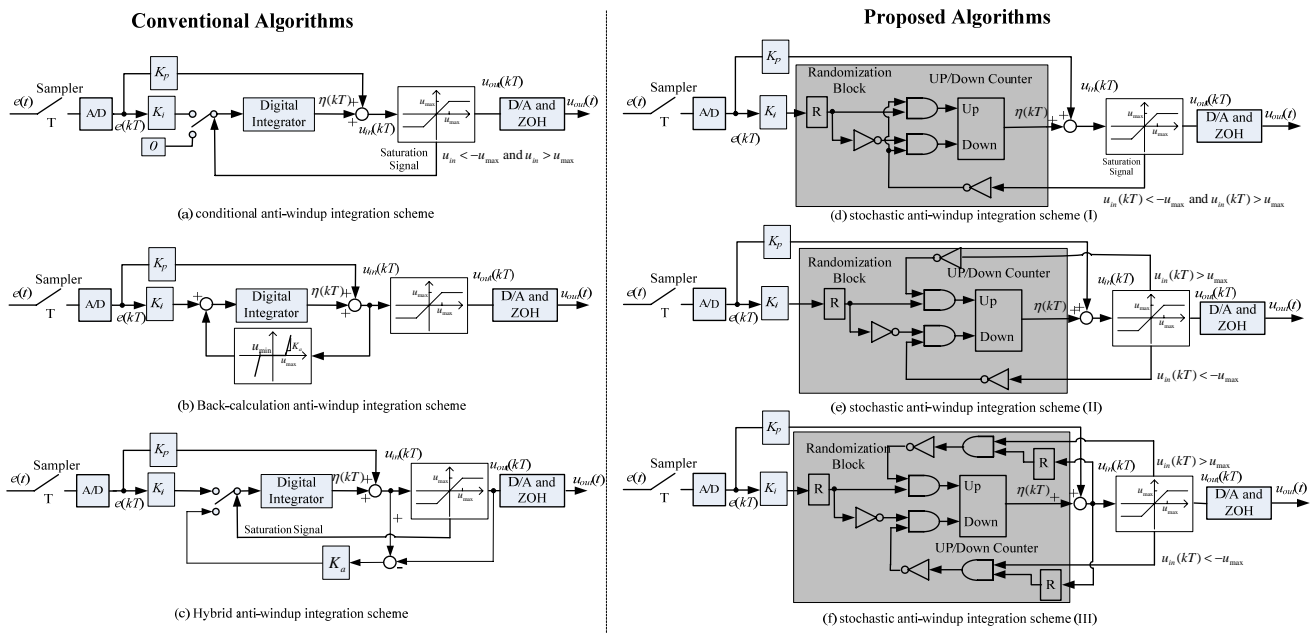


Fig.3 Comparison of the current anti-windup strategies and the proposed strategies

The proposed stochastic anti-windup digital PI control algorithms are illustrated in Fig.3(d), (e), and (f), respectively. In Fig.3(d), the saturation signal is connected to the up/down counter through two AND gates. When the saturation signal is '1', the outputs of the two AND gates both become '0', which disables the accumulation of the up/down counter. The integration process will work as normal when the saturation signal is '0' for the linear region. So this scheme has the same anti-windup function as the conditional anti-windup strategy where the integration action switches off when saturation occurs. In proposed scheme II, shown in Fig.3(e), when the output of the PI controller exceeds the upper limit of the saturator, the AND gate sends out '0' to the up port of the counter and the down port continues to receive the coming pulses. As a consequence, the integral term will decrease which will tend to bring the PI controller back to the linear region. The saturation

occurrence at the lower limit will cause an increase in the magnitude of the integral term and avoid the accumulation of errors. The last proposed scheme shown in Fig.3(f) provides a tuning parameter to adjust the anti-windup performance. The output of the PI controller is randomized to a bit-stream and connected to the saturation signals with AND gates. In this way, when saturation occurs, each of the up and down ports has pulse inputs, but the randomization process decides the rate of the increase or decrease of the integral term. The constant  $C_2$  in the randomization process becomes a free tuning parameter that can be adjusted to optimize the performance. If the output of the integral is defined as  $\eta$ , the derivative of the integral state  $\dot{\eta}$  of each proposed strategy is derived in Table 1 where  $K_i$ , shown in Fig.3 is the integral constant,  $C$  is the constant used in the randomization process in Fig.3(e),  $C_1$  and  $C_2$  are the two different constants used in Fig.3(f) where  $C_1$  is for the randomization at the beginning and  $C_2$  is for the two feedback randomization blocks,  $K_{up} = 1 - u_{in}/C_2$  and  $K_{down} = 1 + u_{in}/C_2$ . Normally, these parameters are chosen based on the range of input data. For the 16-bit resolution,  $C$  and  $C_1$  are normally chosen to be equal or smaller than  $2^{15}$  and  $C_2$  can be chosen between 0 to  $C_1$ .

Table 1 Integral state of the proposed stochastic anti-windup PI controller

Stochastic PI Controllers	The dynamics of the integral state: $\dot{\eta}$		
	$u_{in} = u_{out}$	$u_{in} > u_{out}$	$u_{in} < u_{out}$
Proposed scheme I	$K_i$	0	0
Proposed scheme II	$K_i$	$-K_i C(1 - e/C)/2$	$K_i C(1 + e/C)/2$
Proposed scheme III	$K_i$	$\frac{-K_i C_1 [2(1 - e/C_1) - K_{up}(1 + e/C_1)]}{4}$	$\frac{K_i C_1 [2(1 + e/C_1) - K_{down}(1 - e/C_1)]}{4}$

Fig.4 shows the system diagram of the proposed speed controller applied to the induction motor drives. The speed controller is in either saturation or linear operation mode. In order to demonstrate the stability of the proposed speed controller, the attractivity of the controller transferring from saturation mode to linear mode is investigated. The analysis is focused on the proposed scheme I.

The variable-speed motor drive in Fig.4 is considered as a first-order system since fast current control is assumed. The speed control system therefore is written as:

$$\dot{w}_r = -\frac{1}{\tau_m} w_r + \frac{K_T}{J} u_{out} - \frac{T_L}{J} \quad (1)$$

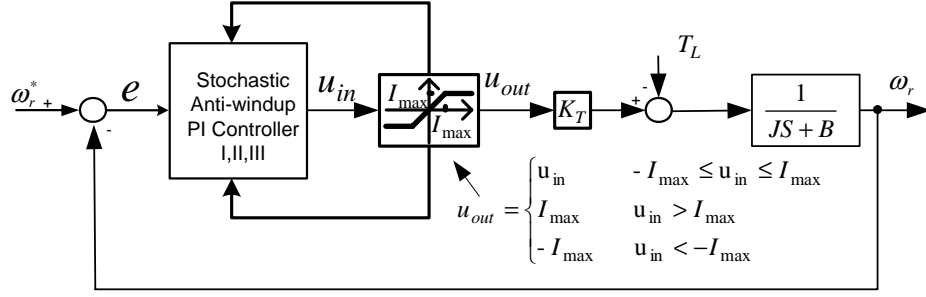


Fig.4 Block diagram of proposed anti-windup PI speed controller

From Fig.3, the output of the PI controller  $u_{in}$  is represented by:

$$u_{in} = K_p \cdot e + \eta \quad (2)$$

By applying the method introduced in [9], the attractive region of the proposed scheme I which guarantee the transfer from saturation mode to linear mode can be derived as followings:

First, by applying speed error:  $e = w_r^* - w_r$  to (2), the derivative of error can be written as:

$$\dot{e} = -\frac{1}{\tau_m} e - \frac{K_T}{J} u_{out} + \frac{1}{\tau_m} w_r^* + \frac{T_L}{J} \quad (3)$$

From Table 1, the derivative of the integral state is 0 which gives:

$$\dot{\eta} = 0 \Rightarrow u_{in} = K_p \cdot e + \eta_C \quad (\eta_C \text{ is constant and is the state when saturation happens})$$

Consider the Lyapunov function:

$$V(e) = \frac{1}{2} e^2 \quad (4)$$

Then, in order to satisfy the attractive condition, the derivative of (4) has to be equal or smaller than 0:

$$\begin{aligned} \dot{V}(e) &= e \cdot \dot{e} = -\frac{1}{\tau_m} e^2 - \frac{K_T}{J} u_{out} e + \frac{1}{\tau_m} w_r^* e + \frac{T_L}{J} e = -\frac{1}{\tau_m} e^2 - \frac{K_T}{J} I_{max} \text{sgn}(u_{in}) e + e \left( \frac{1}{\tau_m} w_r^* + \frac{T_L}{J} \right) \\ &= e \left\{ -\frac{1}{\tau_m} e - \frac{K_T}{J} I_{max} \text{sgn}(K_p \cdot e + \eta_C) + \left( \frac{1}{\tau_m} w_r^* + \frac{T_L}{J} \right) \right\} \leq 0 \end{aligned} \quad (5)$$

Assume  $\eta_C \ll K_p \cdot e$ , the following equation implies the attractive region:

$$-\frac{1}{\tau_m} |e| - \frac{K_T}{J} I_{max} \leq \frac{1}{\tau_m} w_r^* + \frac{T_L}{J} \leq \frac{1}{\tau_m} |e| + \frac{K_T}{J} I_{max} \quad (6)$$

To ensure that the controller will transfer from the saturation mode to the linear mode, the error which defines the attractive region should be in the linear region, so it can get:

$$u_{in} = K_p \cdot e + \eta \Rightarrow \left| K_p \cdot e + \eta \right| \leq I_{max} \Rightarrow -\frac{(I_{max} + \eta)}{K_p} \leq e \leq \frac{(I_{max} - \eta)}{K_p} \quad (7)$$

The attractive condition of the system is calculated based on (6) and (7):

$$-\frac{1}{\tau_m} \left( \frac{(I_{max} + \eta_C)}{K_p} \right) - \frac{K_T}{J} I_{max} \leq \frac{1}{\tau_m} w_r^* + \frac{K_T}{J} \leq \frac{1}{\tau_m} \cdot \left( \frac{(I_{max} - \eta_C)}{K_p} \right) + \frac{K_T}{J} I_{max} \quad (8)$$

The constant integral state  $\eta_C$  is affected by the load torque and time instant when the saturation happens.

### C. Hardware implementation of proposed stochastic anti-windup controller

Fig.5 illustrates the developed digital design scheme of the proposed stochastic anti-windup PI controller I. The other two proposed controllers have the similar structures except the feedback to the up/down counter which is shown in fig.3(e) and (f). The scheme is implemented in a Xilinx FPGA chip using ISE 7.01 software for design, simulation and programming. The controller is written in the VHSIC (Very High Speed Integrated Circuit) Hardware Description Language (VHDL).

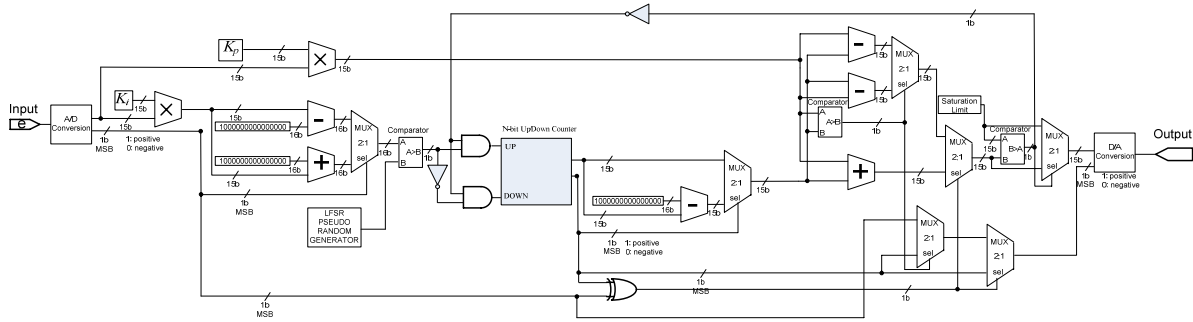


Fig.5 Digital design scheme of stochastic anti-windup PI controller I

## III. HARDWARE-IN-THE-LOOP VERIFICATION

The proposed anti-windup PI speed controllers were applied to the speed control of an induction motor drive using the hardware-in-the-loop test bench shown in Fig.6. The Appendix gives the motor parameters. The power components were simulated using real time digital simulation (RTDS) while the proposed controller was implemented with FPGA. The PI controllers' parameters were initially tuned using experience formula and then improved by trial-and-error to reduce the settling time and maximum overshoot.

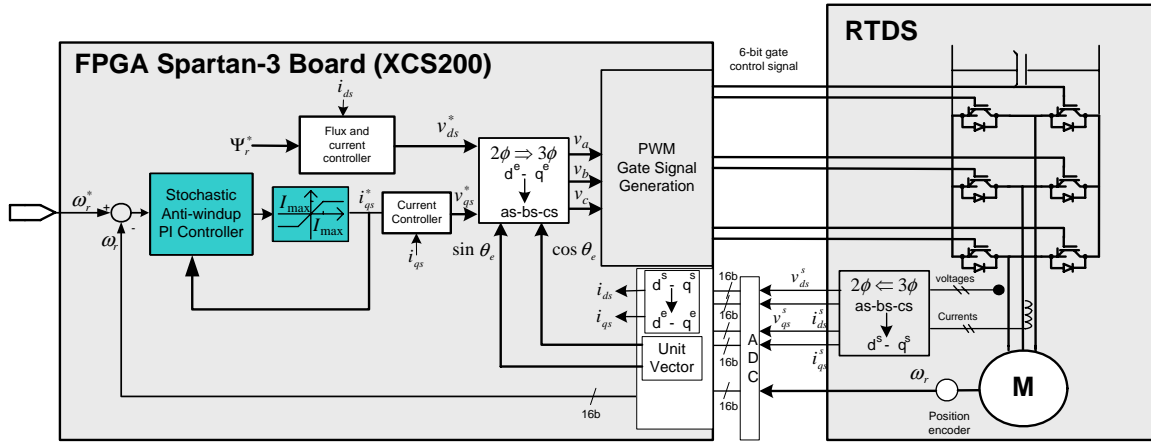
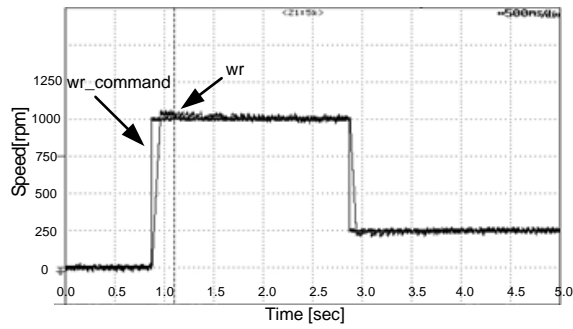
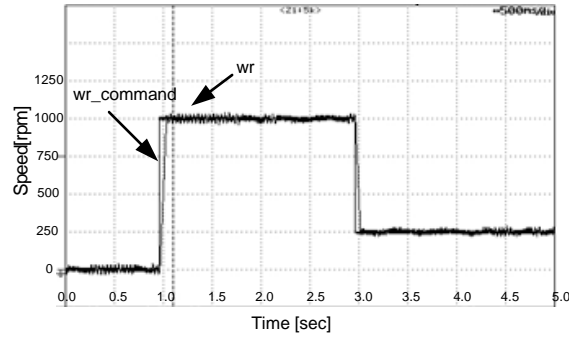


Fig.6 Hardware-in-the loop test setup using FPGA and RTDS

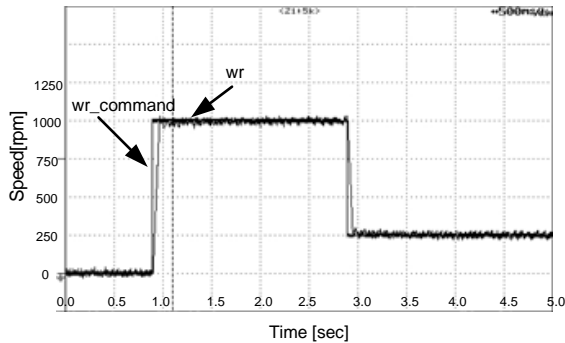
Fig.7 shows the experimental results of the three proposed anti-windup PI speed controllers and the conventional PI controller without anti-windup, respectively. A step command of 1000 rpm was given and then



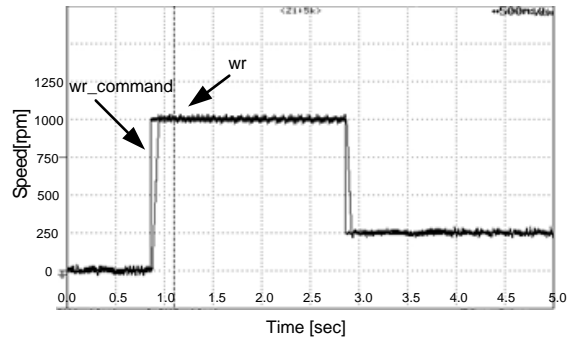
(a) Traditional PI controller without anti-windup technique



(b) Stochastic anti-windup PI controller I



(c) Stochastic anti-windup PI controller II

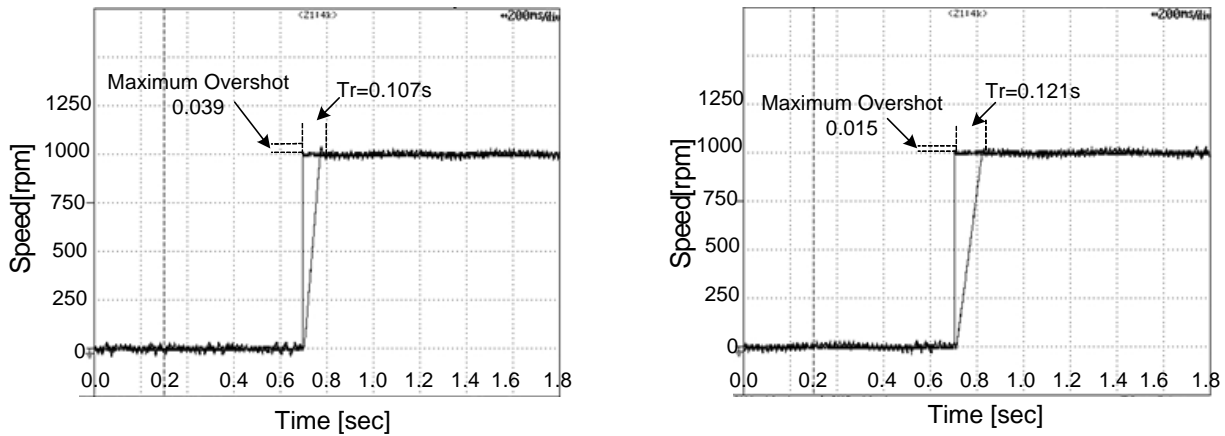


(d) Stochastic anti-windup PI controller III

Fig.7 HIL experimental results of step speed response of proposed controller and conventional controllers reduced to 250 rpm. The developed torque current command was limited to 2.21A. The proportion parameter  $K_p$  is 0.0132 and the integration parameter  $K_i$  is 0.105. As shown in fig.6(a), the lack of an anti-windup mechanism led to the continuous increase of the integral output as long as current command was saturated, which resulted in a large overshoot (0.071) and a long settling time (0.621s). As shown in Fig.7 (b)-(d), the proposed anti-windup

PI control algorithms were used to hold or reduce the integral state when saturation occurred. The control parameters  $C$ ,  $C_1$  and  $C_2$  are chosen to be  $2^{15}$ ,  $2^{15}$  and  $2^{14}$ . The result was that the control performances of the three proposed algorithms yielded improved performance. The maximum overshoot of the three proposed methods are 0.039, 0.033 and 0.029 while the settling time are 0.107s, 0.133s and 0.141s, respectively. From the results, the three proposed methods all improve the control performance and due to the noise effect, further improvement is hard to achieve.

Fig.8 compares the performance of the proposed anti-windup PI controller I with that of the traditional anti-windup PI controller (Fig.2 (a)). The overshoot and settling time are almost the same for the two methods, therefore the proposed algorithm maintains the similar high control performance compared with the conventional anti-windup method.



(a) Proposed stochastic anti-windup PI controller I (Fig.2 (d))

(b) conditional anti-windup PI controller (Fig.2 (a))

Fig.8 HIL experimental results of performance comparison of proposed anti-windup controller and conventional anti-windup controllers

Table 2 illustrates the occupied digital resources by conventional and proposed anti-windup PI controllers for the variable-speed motor drive applications. All the implementations are using FPGA chip - Spartan3 xc3s200 (Xilinx) in VHDL language (ISE 7.01). It shows that the proposed methods save logic cells by 23.1% (proposed method III) –31.0% (proposed method I).

Table 2 Comparison of digital resources used by conventional and proposed anti-windup PI controllers  
Spartan3 xc3s200

Conventional Anti-windup PI controllers		Proposed stochastic Anti-windup PI controllers	
Types	Used Number of Slices	Types	Used Number of Slices
Condition	100	I	69
Back-calculation	107	II	75
Hybrid	121	III	93

## IV. CONCLUSION

This paper presents three stochastic anti-windup PI algorithms and their digital implementations by FPGA based on stochastic theory. The stability conditions are investigated. The proposed control schemes have been applied to the speed control of a vector-controlled induction motor drive using a hardware-in-the-loop test bench. The resulting control performances are compared with those of PI without anti-windup and conventional anti-windup PI controllers. This comparison results confirms that the proposed controllers are able to achieve the high control performance of traditional anti-windup schemes with reduced digital resources and simplified design process.

### Appendix

#### Nomenclature:

B Friction coefficient	J Moment of inertia of total system
K Proportional gain of the PI controller	$K_T$ Torque constant
$\eta$ Integral state of the PI controller	$T_I$ Integral time constant of the PI controller
$T_L$ Load Torque	$\tau_m$ Mechanical time constant (= J/B)
$u_{out}$ Output of the Limiter	$u_{in}$ Input of the Limiter
$w_r$ Motor rotor speed	$w_r^*$ Motor rotor speed command

#### Parameters of induction motor:

Power Rating	1 hp	Number of poles	2
Stator resistance	2.99 $\Omega$	Stator inductance	3.46 $\cdot 10^{-3}$ H
Rotor resistance	1.58 $\Omega$	Rotor inductance	1.37 $\cdot 10^{-3}$ H
Magnetizing inductance	60.41 $\cdot 10^{-3}$ H	Base frequency	60 Hz
Moment of inertia	0.0012kg $\cdot m^2$		

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